IMPACT
International Microsystems, Packaging, Assembly and Circuits Technology conference

Thermal and Reliability-Oriented Structural Optimization of IMS Substrates for Power Module Applications

Tsung-Han Li[1], Pouria Zaghari[3], Yu-Jen Wang[1], Jen-Kuang Fang [2],Jen-Chun Chen[2], Pai-Sheng Shih[2], Jong Eun Ryu[3], Fuh-Gwo Yuan[3]

[1]Institute of Advanced Semiconductor Packaging and Testing, National Sun Yat-sen University

No. 70, Lianhai Rd., Gushan Dist., Kaohsiung City 80424, Taiwan (R.O.C.)

[2]Advanced Semiconductor Engineering Inc.

No. 26, Jing 3rd Rd., Nanzi Dist., Kaohsiung City 811641, Taiwan (R.O.C.)

[3]Department of Mechanical and Aerospace Engineering, North Carolina State University

1840 Entrepreneur Drive, Raleigh, NC 27606, USA

m12a010071@g-mail.nsysu.edu.tw[1]

ABSTRACT

To address thermo-mechanical challenges in power module substrates, this study investigates three Insulated Metal Substrate (IMS) designs with varied copper layer thicknesses. Finite element analysis (FEA) was employed to predict thermal resistance and mechanical warpage, followed by experimental validation through warpage measurements and dielectric insulation tests. The objective is to identify an optimal IMS configuration that balances thermal performance with mechanical reliability, thereby providing a robust substrate solution for next-generation power electronics.

INTRODUCTION

The rapid adoption of electric vehicles (EVs) continues to drive stringent requirements for thermal management, reliability, and cost efficiency in power module packaging [1]. Ceramic substrates such as Direct Bonded Copper (DBC) and Active Metal Brazed (AMB) remain widely used due to their high thermal conductivity and strong insulation. However, the coefficient of thermal expansion (CTE) mismatch between ceramic and copper layers often induces warpage, delamination, and edge chipping, which restrict layout flexibility and necessitate symmetric thickness designs [2].

In contrast, IMS substrates-owing to the closer CTE compatibility between the dielectric and metal base-offer greater design flexibility, including the use of asymmetric copper thickness configurations [3]. Furthermore, IMS designs enable optimization of the dielectric layer to reduce thermal resistance and improve heat spreading [4]. Nevertheless, ensuring insulation robustness remains essential, as breakdown and partial discharge (PD) related degradation at the module level directly influence substrate stack-up selection and qualification testing [5].

Accordingly, this work investigates three IMS designs (symmetric copper, thicker top copper, and thicker bottom copper), integrating FEA-based thermal and warpage predictions with experimental validation of warpage behavior and insulation performance.

EXPERIMENTAL AND SIMULATION METHODS

Substrate Structure Design

This study evaluates the thermo-mechanical performance of six power module substrates, divided into two categories: conventional ceramic substrates and IMS. The ceramic group comprises a Zirconia-Toughened Alumina (ZTA) DBC substrate and two AMB substrates, both using Silicon Nitride (Si_3N_4) from different suppliers (designated as H and K, respectively). While the two AMB variants share identical stack-up dimensions, they differ in material properties.

The IMS group consists of three designs with varied copper layer configurations to assess the influence of structural asymmetry. All substrates share the same lateral dimensions of 45.5 mm × 32.7 mm and a total thickness of 1.3 mm. Detailed stack-up parameters and schematic diagrams for each sample are provided in Table 1 and Figure 1.

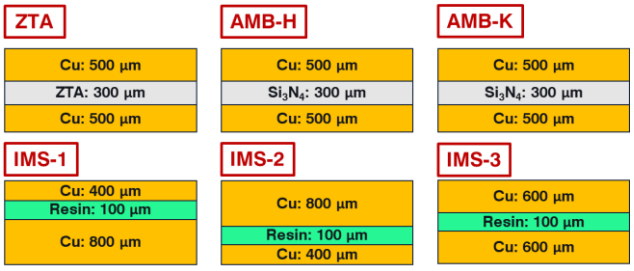


Figure. 1. Schematic cross-sections of the substrate stack-up designs: ZTA, AMB, and the three IMS configurations.

Table I. Structural parameters of the evaluated power module substrates.

Dielectric Material	Thickness (Cu/Dielectric/Cu)
Si_3N_4	0.5/0.3/0.5 mm
Al_2O_3-ZrO_2	0.5/0.3/0.5 mm
Resin	0.4/0.1/0.8 mm
	0.8/0.1/0.4 mm
	0.6/0.1/0.6 mm

Finite Element Analysis (FEA)

A full-model 3-D finite element analysis (FEA) was carried out using ANSYS to evaluate the thermal and mechanical behavior of the substrates. The models were discretized using a combination of fine tetrahedral and hexahedral elements, resulting in approximately 156,992 elements, as illustrated in Figure 2(a). The material properties employed in the simulations-including those of copper, IMS resin, ZTA, and the two types of Si_3N_4 are summarized in Table 2. To improve the accuracy of warpage predictions, temperature-dependent properties were incorporated into the analysis.

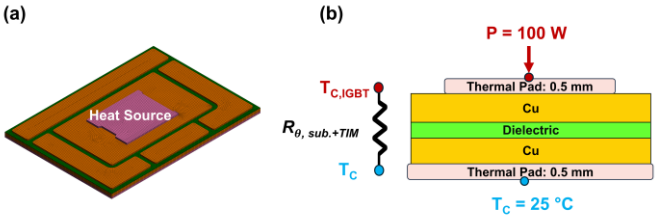


Figure 2. (a) 3-D finite element model and corresponding mesh structure used in the analysis. (b) Boundary conditions for thermal resistance estimation and the equivalent thermal resistance circuit.

Table II. Material properties used in the finite element simulations.

Property (Unit)	Copper	IMS Resin	Al_2O_3-ZrO_2	Si_3N_4-H	Si_3N_4-K	Thermal Pad
Thermal Conductivity (W/m·K)	395	10	25	80	80	6
Young's Modulus (GPa)	110.23-0.0496T	30	310	280	310	—
Poisson's Ratio	0.34	0.1	0.24	0.28	0.34	—
Coefficient of Thermal Expansion (ppm/°C)	16.34+0.0063T	11.7	7.5	2.6	2.5	—
Yield Strength (MPa)	19.26-0.0103T	—	—	—	—	—
Tangent Modulus (GPa)	1.132-0.0013T	—	—	—	—	—

Thermal Simulation

To assess thermal performance, a steady-state thermal analysis was performed. A heat load of 100 W, corresponding to the power dissipation of a 15 mm × 12.5 mm silicon (Si) IGBT die, was uniformly applied to the thermal pad region on the substrate's top surface (Figure 2(b)). The bottom surface of the substrate was fixed at a constant temperature of 25 ℃ to emulate an ideal heatsink condition. By performing the thermal finite element analysis and deriving the temperature distribution, the thermal resistance of the structure ($R_{\theta,sub.+TIM}$) can then be estimated.

Warpage Simulation

Mechanical warpage of the substrate was investigated through a static structural analysis coupled with thermal loading. The simulation reproduced a typical solder reflow process, in which the substrate temperature was ramped from 25 ℃ to 260 ℃ and subsequently cooled back to 25 ℃, as illustrated in Figure 3. The analysis focused on predicting total deformation and out-of-plane displacement (warpage) at room temperature following the thermal cycle. The mechanical boundary conditions for the warpage analysis are provided in Figure 3. The 3-D substrate structure and the mechanical boundary conditions for the warpage analysis are presented in Figure 3(a-b). As shown, to prevent rigid-body motion while allowing the inherent warpage of the substrates to develop, three nodes of the bottom copper layer were constrained.

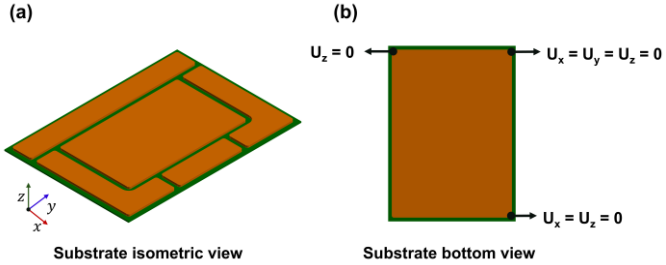


Figure. 3. (a) Substrate 3-D and (b) mechanical boundary conditions for warpage simulation.

Experimental Warpage Measurements

Warpage measurements were conducted using an Akrometrix PS400 Shadow Moiré system. For each substrate group, five samples (n=5) were evaluated. The samples were subjected to the same temperature profile applied in the FEA simulations, i.e., heating from 25 ℃ to 260 ℃ followed by cooling back to 25 ℃, at a ramp rate of approximately 0.5 ℃/s, as shown in Figure 4. Full-field warpage was continuously monitored and recorded throughout the thermal cycle.

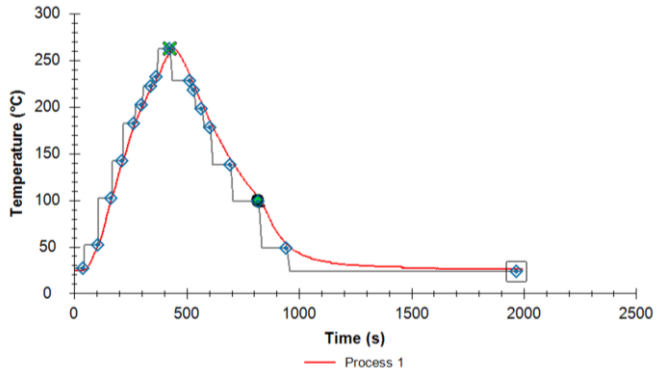


Figure 4. Temperature profile used for warpage measurement

Insulation Performance Test

The dielectric strength of the substrates was evaluated using a dielectric breakdown test in accordance with ASTM D149. An Associated Research HypoTMAX® 7715 AC Withstand Voltage Tester was employed for the measurements. For each substrate group, five samples (n=5) were tested. An AC voltage was applied at a constant ramp rate of approximately 200 V/s until breakdown occurred, which was defined as the point where the leakage current reached or exceeded 10.0 mA.

RESULT AND DISCUSSION

Thermal Performance Simulation Analysis

The steady-state thermal simulation results for all substrate designs are summarized in Table III. For clarity, the results for the best-performing ceramic substrate (AMB, Si_3N_4) and the highest-performing IMS design are highlighted. The data show that the AMB substrate achieved the lowest thermal resistance (0.690 K/W), indicating the most efficient heat dissipation. In contrast, the ZTA DBC substrate exhibited the highest thermal resistance (0.721 K/W),

primarily due to the relatively lower thermal conductivity of its ceramic layer.

Table III. Steady-state thermal simulation results for substrate designs.

Dielectric	Size (Cu/Dielectric/Cu)	$T_{C,IGBT}$ (°C)	$R_{\theta,sub.+TIM}$ (K/W)
Resin (IMS)	0.4/0.1/0.8 mm	95.3	0.703
	0.8/0.1/0.4 mm	**94.8**	**0.698**
	0.6/0.1/0.6 mm	94.9	0.699
Si_3N_4	**0.5/0.3/0.5 mm**	**94.0**	**0.690**
Al_2O_3-ZrO_2	0.5/0.3/0.5 mm	97.1	0.721

Among the three IMS configurations, the design with the thickest top copper layer (0.8/0.1/0.4 mm) exhibited the best thermal performance ($R_{\theta,sub.+TIM}$ = 0.698 K/W). This improvement is attributed to enhanced lateral heat spreading by the thick top copper, which mitigates heat concentration at the source before thermal energy passes through the lower-conductivity resin layer. A representative temperature distribution for an IMS substrate is shown in Figure 5.

Interestingly, although the Si_3N_4 ceramic (k=80 W/m·K) is substantially more conductive than the IMS resin (k=10 W/m·K), its greater required thickness (300 µm vs. 100 µm) reduces this advantage. Consequently, the top-performing IMS design exhibits a thermal resistance only slightly higher than that of the AMB substrate (0.698 K/W vs. 0.690 K/W), demonstrating the effectiveness of the thin-dielectric IMS architecture for high-performance thermal management.

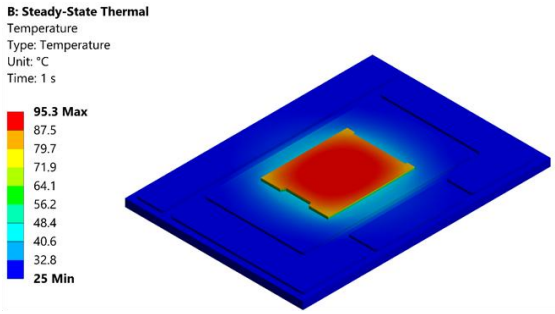
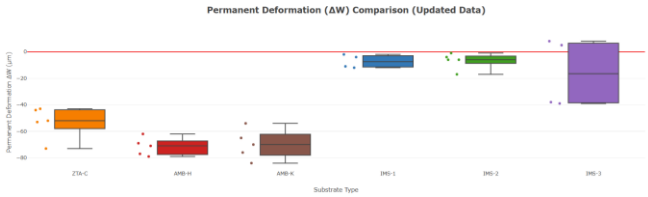


Figure 5. Simulated temperature distribution of the IMS-1 substrate from the steady-state thermal analysis.

Experimental Warpage Results

The permanent deformation (ΔW) of all six substrate types following a simulated reflow cycle was experimentally characterized to evaluate their thermo-mechanical reliability. The statistical distribution of the results is presented in the box plot shown in Figure 6. The data reveal a pronounced contrast in performance between the conventional ceramic substrates and the IMS designs.

The ceramic substrates exhibited substantial post-cycle residual warpage. The ZTA-C substrate showed an average permanent deformation of -53.0 µm, whereas the AMB substrates performed even worse, with AMB-H and AMB-K samples reaching -71.6 µm and -69.8 µm, respectively. These large negative deformations (concave warpage) indicate significant residual stress accumulated during the thermal cycle. Moreover, with peak warpage values exceeding 160 µm for ZTA and 240 µm for AMB during the cycle (as illustrated for a representative sample in Figure 7), these substrates present a considerable process risk during assembly.



Permanent Deformation (ΔW) Data (Updated)

Substrate Type	Average ΔW (µm)
ZTA-C	-53.0
AMB-H	-71.6
AMB-K	-69.8
IMS-1	-7.3
IMS-2	-6.8
IMS-3	-27.5

Figure. 6. Box plot of permanent deformation (ΔW) for all substrate types following a simulated reflow cycle.

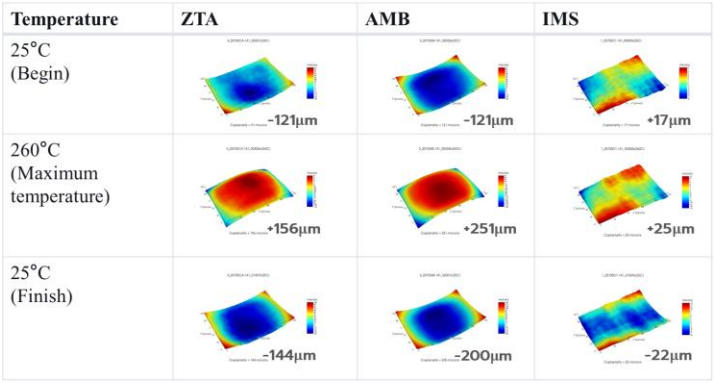


Figure 7. Evolution of warpage maps for representative ZTA, AMB, and IMS substrates at key temperatures (initial 25 °C, peak 260 °C, and final 25 °C) during a simulated reflow cycle

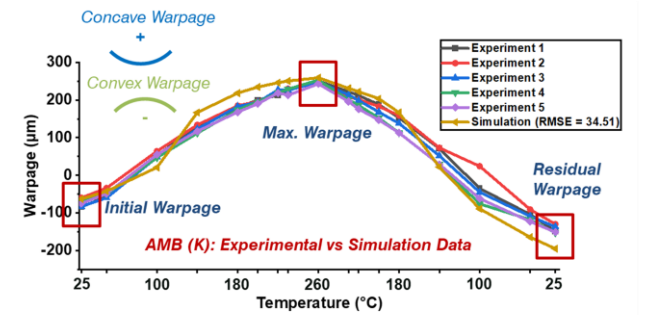
In stark contrast, all three IMS designs demonstrated exceptional thermo-mechanical stability. Both the IMS-1 and IMS-2 designs recorded a near-zero average permanent deformation (-7.3 µm and -6.8 µm, respectively), which is an order of magnitude lower than their ceramic counterparts. With peak warpage remaining below 40 µm, the IMS series exhibits high potential for both superior reliability and high-yield manufacturability, making them the only recommended substrate type for this application.

Among the IMS series, the asymmetric IMS-2 (thicker-top copper) design showed the most consistent and lowest deformation, positioning it as the most robust option for immediate implementation. While the symmetric IMS-3 was theoretically expected to perform best, its data showed wider variation, potentially due to measurement noise at near-zero warpage levels, warranting further investigation.

Simulation Model Validation

To ensure the predictive accuracy of the FEA model, a parametric study was conducted to calibrate temperature-dependent material properties, with particular focus on the plastic behavior of copper. The AMB (KCC) substrate served as the benchmark for this validation.

As shown in Figure 8, the simulated warpage–temperature curve exhibits excellent agreement with the five experimental measurement curves over the entire reflow cycle. The model accurately reproduces key behaviors, including initial warpage, peak convex warpage near 260 °C, and final residual warpage at room temperature. Numerical comparison indicates a maximum warpage prediction error of only 4.3%, with an overall Root Mean Square Error (RMSE) of 34.51 μm, confirming the model's high fidelity. With this level of accuracy, the model can be confidently employed to compare the thermo-mechanical performance across all substrate designs.



Warpage (μm)	Simulation	Experiment						Error %
	Best Fit	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Average	
Initial Warpage	-63	-84	-60	-83	-69	-75	-74.2	15.1%
Max. Warpage	259	251	247	248	253	243	248.4	4.3%
Residual Warpage	-195	-149	-130	-137	-153	-151	-144.0	35.4%

Figure 8. Comparison of warpage simulation versus five experimental measurements for the AMB-K substrate.

Insulation Strength Analysis

The dielectric strength of each substrate was assessed via breakdown voltage tests, with the results summarized in Table IV. The data indicate that the ceramic substrates, particularly AMB-H (9.50 kV) and ZTA-C (8.78 kV), exhibit the highest absolute dielectric strength. In comparison, the IMS series showed lower breakdown voltages, ranging from 4.30 kV to 4.87 kV.

Notably, despite featuring an insulation layer only one-third the thickness of the ceramic substrates, all IMS designs comfortably exceed the required test voltage (typically 2.5–4.0 kV) specified by IEC 61800-5-1 for 1200 V-class power modules. This demonstrates that the thin-dielectric IMS architecture provides sufficient insulation for high-voltage applications, offering an adequate safety margin.

Table IV. Summary of measured dielectric breakdown voltage data.

Substrate Type	Sample ID	VoltageBreakdown / Test Voltage (kV)	Average Breakdown (kV)
ZTA-C	1	8.75	8.78
	2	8.97	
	3	8.61	
AMB-H	1	9.70	9.50
	2	9.56	
	3	9.24	
AMB-K	1	5.54	6.21
	2	6.53	
	3	6.55	
IMS-1	1	3.73	4.30
	2	4.55	
	3	4.63	
IMS-2	1	4.57	4.87
	2	4.95	
	3	5.08	
IMS-3	1	3.85	4.39
	2	4.62	
	3	4.71	

CONCLUSION

This study provides a systematic comparison of Insulated Metal Substrates (IMS) against conventional ceramic substrates (DBC/ZTA, AMB/Si_3N_4) under identical total thickness conditions, integrating both simulation and experimental validation. The key findings are threefold:

1. Thermal Performance: IMS designs employing a thin-dielectric, thick-copper architecture optimizes the heat transfer path. Notably, the asymmetric "thicker-top copper" design (IMS-2) achieves a thermal resistance comparable to high-conductivity AMB substrates, owing to its superior lateral heat spreading.

2. Mechanical Reliability: Shadow Moiré measurements indicate that the post-reflow permanent warpage of all IMS designs is significantly lower than that of conventional ceramic substrates, demonstrating excellent thermo-mechanical stability.

3. Insulation Performance: Despite the reduced dielectric thickness, the breakdown voltage of all IMS samples comfortably exceeds the requirements of relevant international standards, providing adequate safety margins.

In summary, this work confirms that IMS (particularly the asymmetric thicker-top copper design) is a highly viable option for future power module substrates. Future efforts will focus on completing experimental thermal resistance measurements (including power cycling) and continuously calibrating the FEA model with empirical data. The ultimate goal is to establish a predictive simulation platform, formulate optimal design rules, and validate module-level reliability using the optimized substrate.

ACKNOWLEDGEMENT

The authors gratefully acknowledge TCLAD Inc. for support in sample fabrication, Professor Fuh-Gwo Yuan of National Cheng Kung University for introducing the MAE team at North Carolina State University, and said team for their essential assistance with the FEA simulations.

REFERENCES

[1] F. Blaabjerg *et al.*, "Reliability of Power Electronic Systems for EV/HEV Applications," *Proc. IEEE*, vol. 109, no. 6, pp. 1060–1076, June 2021.

[2] S. Zhang *et al.*, "Residual stress and warpage of AMB ceramic substrate studied by finite element simulations," *Microelectron. Reliab.*, vol. 98, pp. 49–55, July 2019.

[3] E. Gurpinar *et al.*, "Design, Analysis, Comparison, and Experimental Validation of Insulated Metal Substrates for High-Power Wide-Bandgap Power Modules," *ASME J. Electron. Packag.*, vol. 142, no. 4, Paper no. JEP-20-1056, Dec. 2020.

[4] W. Fan *et al.*, "Improving Heat Conduction of Insulated Metal Substrate with Thermal Pyrolytic Graphite Core for SiC Power Module Packaging," *Mater. Sci. Forum*, vol. 1004, pp. 1022–1027, 2020.

[5] L. Xu *et al.*, "Analysis of Discharge Failure Mechanism of IGBT Power Module," *Energies*, vol. 16, no. 16, p. 6001, Aug. 2023.