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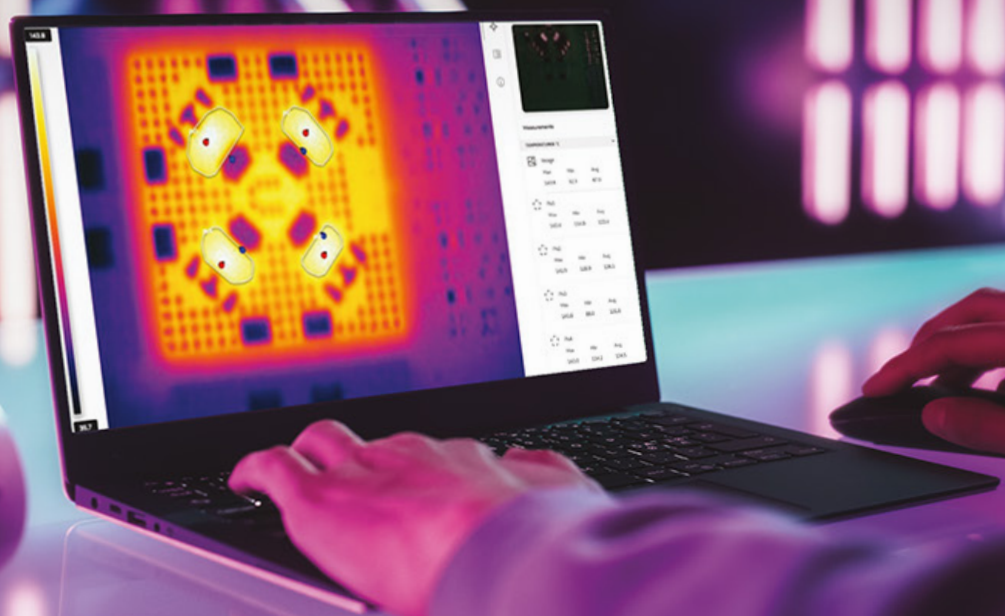
Thermal Bridges

Managing Heat in Power-Dense Electronics



Flex Material Selection

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THERMAL
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Experimental Evaluation of High-Thermal Dielectric Materials and Surface-Mount Thermal Bridges in Multilayer PCB Designs

A study shows how high-thermal dielectrics outperform FR-4 for bulk heat spreading, with surface-mount thermal bridges serving as targeted tools for hotspot control.

BY CHRIS PARKER, MARTIN ANSLEM, PH.D., AND FRANCISCO AGUILAR

As power density continues to increase across power electronics, industrial controls, automotive electrification and data center infrastructure, printed circuit boards (PCBs) are increasingly required to function as active thermal management structures rather than passive interconnect platforms. Localized hotspots, rising junction temperatures and constrained form factors are pushing conventional FR-4 substrates beyond their practical thermal limits. In response, PCB designers are adopting a combination of material-level improvements within the PCB stackup and localized heat-spreading solutions. One such approach is the use of surface-mount thermal bridges (SMTBs), passive SMT components designed to conduct heat away from power devices and redistribute it into larger copper regions of the PCB without providing an electrical function.

This study presents a controlled experimental comparison between standard FR-4 and an advanced high-thermal dielectric PCB material, evaluated both with and without SMTBs. Identical six-layer test vehicles were designed, fabricated and assembled, and then tested under repeatable power-cycling conditions at Rochester Institute of Technology (RIT). Thermal performance was quantified using infrared (IR) thermography, with validation through thermocouple measurements. Multiple experimental iterations were conducted to examine the effects of substrate material, SMTB presence, SMTB size and overall board temperature on thermal behavior.

Results show that boards fabricated with the advanced thermal dielectric consistently operated at lower temperatures than FR-4 across all quadrants and test configurations. SMTBs provided measurable reductions in peak component temperature on both substrates; however, their relative impact diminished on the higher-performance dielectric, indicating that bulk heat spreading through the PCB material becomes the dominant thermal pathway as substrate conductivity improves. These findings support the use of advanced thermal dielectric materials as drop-in replacements for FR-4 in high-power designs and position SMTBs as a complementary, fine-tuning thermal solution for managing localized hotspots.

Thermal Challenges in High-Power Designs

Electronic systems are undergoing a sustained increase in power density driven by electrification, automation and high-performance computing. Power conversion stages, motor drives, battery management systems and AI accelerators now concentrate significant heat generation into increasingly compact footprints. In many of these systems, the PCB itself is required to dissipate a substantial portion of this heat, particularly when airflow is limited or mechanical heat sinking is constrained.

Traditional PCB thermal management strategies, such as increasing copper weight, adding thermal vias or attaching external heat sinks, are often insufficient to address localized hotspots at the component level. These approaches may reduce average board temperature but frequently fail to prevent excessive junction temperatures in high-power surface-mount devices. As a result, designers are increasingly exploring material-level solutions within the PCB stackup.

Surface-mount thermal bridges (SMTBs) are passive SMT components used to reduce localized hotspot temperatures in surface-mount power devices. They are mounted on the PCB using standard assembly processes and serve no electrical function. Instead, SMTBs create a low thermal resistance path that conducts heat away from a hot component and distributes it to larger copper areas of the board, thereby increasing the effective heat-spreading area.

During operation, heat flows from the component pad into the SMTB and is redistributed into connected copper planes, thermal vias or other heat-spreading features within the PCB stackup. This reduces thermal bottlenecks at the component interface and lowers peak device temperatures. Because SMTBs rely on conduction rather than airflow, they are well-suited for compact, enclosed or passively cooled systems.

The effectiveness of an SMTB depends strongly on the thermal performance of the PCB material. On conventional FR-4, SMTBs can provide meaningful temperature reductions by compensating for limited heat spreading in the dielectric. As part of a thermal design strategy, SMTBs are most effective when used as a complementary solution alongside appropriate substrate selection and PCB layout optimization.

Substrates Comparison

FR-4 remains the dominant PCB substrate due to its balance of cost, electrical performance, mechanical stability and compatibility with standard fabrication and assembly processes. However, FR-4 has a relatively low thermal conductivity, typically on the order of 0.3 – 0.4 W/m·K, which limits its ability to spread heat both laterally within copper layers and vertically through the board thickness. As component power density increases, this limitation results in steep local temperature gradients, elevated junction temperatures and reduced thermal margin at the device level. In high-power surface-mount applications, these effects

can accelerate failure mechanisms such as solder joint fatigue, dielectric aging and reduced semiconductor lifetime.

High-thermal-dielectric materials such as the novel SFL-12, with a through-plane thermal conductivity of approximately 12 W/m·K, provide a substantial improvement in bulk heat dissipation compared with standard FR-4. In the RIT study, identical six-layer test vehicles fabricated with SFL-12 consistently operated at significantly lower temperatures than their FR-4 counterparts under the same power-cycling conditions.

From a design perspective, these quantitative differences translate directly into increased thermal headroom and improved reliability margins. A 26°C reduction in peak temperature can significantly extend component lifetime and enable higher allowable power dissipation within the same board footprint. By improving heat transfer through the PCB stackup rather than relying solely on copper geometry or localized thermal features, high-thermal dielectrics can reduce thermal bottlenecks at the material level.

Advanced high-thermal-dielectric materials are engineered to enhance heat transfer without compromising electrical isolation or mechanical stability. When combined with localized heat-spreading elements such as surface-mount thermal bridges, these materials offer a hybrid approach that addresses both bulk heat spreading and hotspot mitigation.

Thermal Physics of Heat Dissipation

Heat dissipation in multilayer printed circuit boards is governed by the balance between in-plane heat spreading within copper layers and through-plane heat conduction across dielectric layers. While copper planes provide very high in-plane thermal conductivity, their ability to remove heat from a surface-mounted power device is limited by the efficiency with which heat can conduct vertically through the dielectric into those planes. In conventional FR-4 constructions, the low dielectric thermal conductivity creates a dominant thermal resistance in the heat-flow path, causing heat to remain concentrated near the component and resulting in elevated junction and case temperatures. Once this dielectric bottleneck is reached, further increases in copper weight or plane area offer diminishing thermal benefit.

The measured 26°C reduction in peak component temperature observed in quadrant 1 directly reflects the impact of improving this through-plane thermal path. By replacing FR-4 (≈0.3 – 0.4 W/m·K) with a high-thermal dielectric material (≈12 W/m·K), the dominant thermal resistance in the stackup is substantially reduced, permitting heat to flow more efficiently away from the component and into internal copper layers and surrounding board structures. From a thermal physics standpoint, this shifts the heat-transfer regime from localized conduction near the component interface to bulk heat spreading through the PCB, resulting in lower peak temperatures even in the absence of additional localized thermal features such as surface-mount thermal bridges.

This same mechanism explains why the relative benefit of surface-mount thermal bridges diminishes on high-thermal dielectric substrates. On FR-4, SMTBs provide an alternate conduction path that partially compensates for poor dielectric heat transfer and produces measurable temperature reductions. However, once the dielectric itself enables efficient vertical heat flow, as evidenced by a 26°C reduction in baseline temperature, the PCB stackup becomes the primary heat-spreading element. In this regime, SMTBs contribute only incremental improvements by fine-tuning local heat distribution rather than overcoming a fundamental material limitation **(Figure 1)**. These results reinforce a substrate-first thermal design approach, where improvements in dielectric thermal conductivity yield the largest temperature reductions, and localized thermal solutions serve as secondary optimization tools.

Figure 1. Quadrant 1 of FR-4 with no SMTBs.

Study Objectives

The primary objective of this study was to experimentally validate the thermal performance improvements achieved by using a high-thermal-dielectric prepreg laminate stackup compared with a standard FR-4 baseline. The study was designed to quantify the effect of enhanced dielectric thermal conductivity on heat dissipation within a multilayer PCB under controlled operating conditions. In addition, the work aimed to evaluate the effectiveness of SMTBs as a localized thermal management strategy when combined with high-thermal-conductivity dielectric materials.

To achieve these objectives, the study focused on the following specific goals:

- Quantitatively compare the steady-state and transient thermal behavior of electrically and mechanically identical FR-4 and high-thermal prepreg test boards
- Evaluate the temperature reduction achieved through use of SMTBs on both standard and high-thermal dielectric substrates
- Assess the influence of SMTB size and placement on peak component temperature.

Experimental test vehicle design. Two electrically identical six-layer PCBs were fabricated for this study: one using standard FR-4 materials and the other using a high-thermal-dielectric prepreg laminate **(Figure 2)**. The boards were designed with the same layer count, copper weights and finished thickness in order to isolate the impact of dielectric thermal performance on overall heat dissipation.

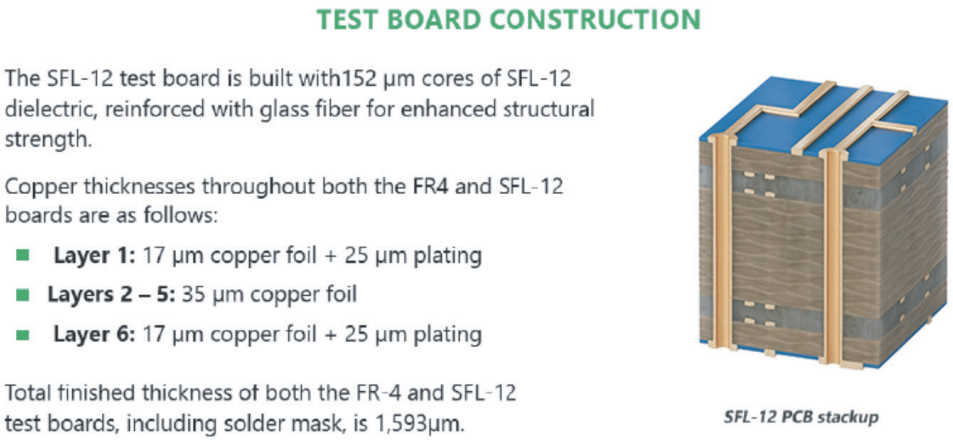

Figure 2. Test board construction and SFL-12 PCB stackup.

Each board incorporated 152 µm dielectric core layers reinforced with glass fiber, resulting in a total finished thickness of approximately 1.6 mm, including solder mask. Copper thicknesses were held constant across both material sets, with plated outer layers and uniform copper distribution on the internal layers, ensuring that any observed thermal performance differences could be attributed primarily to the dielectric and prepreg materials rather than variations in copper geometry or board construction.

The test vehicles were designed using established PCB thermal management techniques, including heavy copper layers and strategically placed thermal vias, to promote efficient heat dissipation. Component placement within each quadrant was intentionally arranged to create localized thermal hotspots while preserving symmetry across the board.

This symmetrical layout ensured consistent thermal boundary conditions across all quadrants, enabling direct and repeatable comparison of thermal performance between different dielectric materials and test configurations without introducing layout-driven bias.

Surface-mount thermal bridge configurations. Three SMTB designs were evaluated, representing a range of thermal resistances and package constructions. These bridges were mounted adjacent to the power devices and connected to dedicated copper planes intended to spread heat laterally and through the board thickness.

Different experimental phases evaluated boards with no thermal bridges, one thermal bridge per quadrant, and two thermal bridges per quadrant to study scaling effects.

Test environment and fixture design. All testing was conducted at RIT using a custom fixture designed to ensure repeatable positioning, airflow isolation and consistent infrared thermal imaging. A fixed gap was maintained between the PCB and IR camera to minimize measurement variability. Ambient temperature was monitored throughout testing and remained stable across all trials.

Each test followed a standardized 20-minute cycle consisting of a 14-minute powered-heating phase, followed by a 6-minute unpowered cooldown phase. This protocol enabled evaluation of both transient heating behavior and near-steady-state conditions. Multiple trials were conducted for each quadrant and configuration to establish repeatability.

Thermal data were captured using a calibrated FLIR infrared camera, with images recorded at 30-second intervals throughout each test cycle **(Figure 3)**. Component temperatures were extracted from the infrared images and plotted as a function of time to evaluate both transient and steady-state thermal behavior.

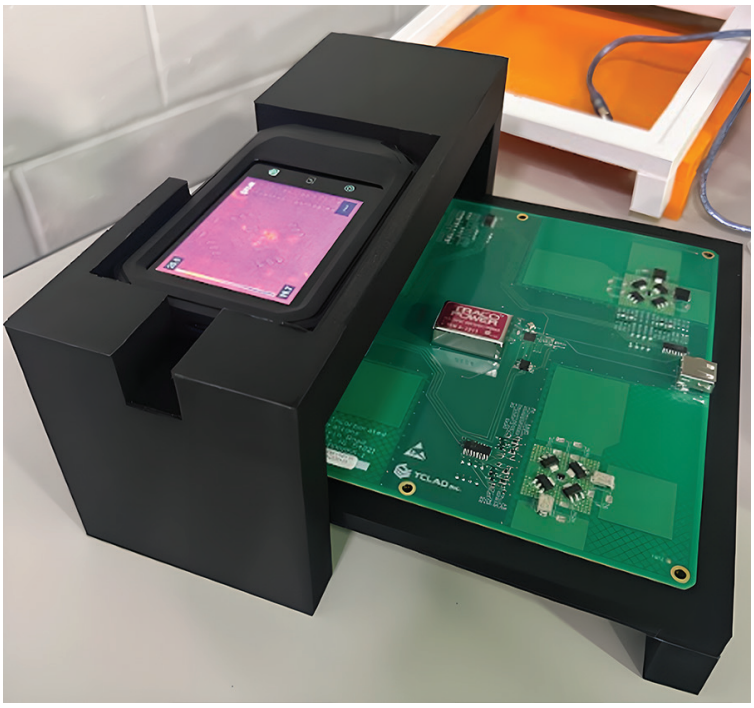

Figure 3. Design test fixture with FLIR mounted above test board.

To validate the infrared measurements, a subset of experiments incorporated K-type thermocouples attached directly to selected transistors. Thermocouple data were logged simultaneously with IR imaging, enabling direct comparison of the measurement methods and the identification of systematic offsets, while confirming overall thermal trends.

Infrared measurements consistently reported slightly higher absolute temperatures than thermocouples. Relative trends between materials and configurations remained consistent across both measurement techniques, however.

To instill confidence in the experimental results, thermal measurements were obtained using both infrared (IR) thermography and direct-contact thermocouples, allowing cross-validation of the observed temperature trends. The FLIR infrared camera provided noncontact, spatially resolved temperature data across the test vehicles, enabling consistent identification of peak component temperatures during both transient heating and near-steady-state conditions **(Figures 4 and 5)**. To verify the accuracy of these measurements, K-type thermocouples were attached directly to selected power transistors and logged simultaneously with IR data under identical power-cycling conditions. This dual-measurement approach ensured that observed temperature differences between materials and test configurations were not artifacts of a single measurement technique.

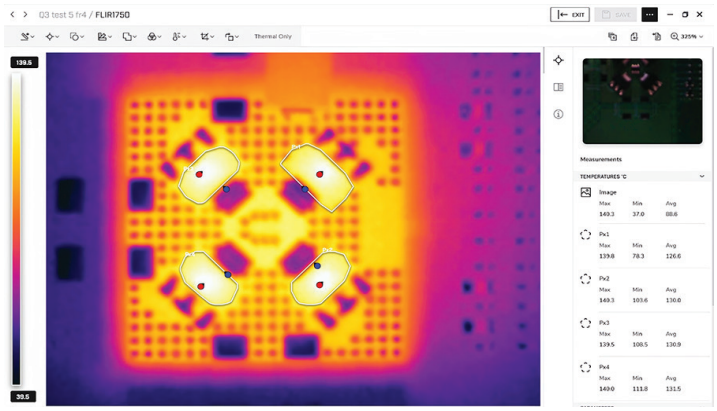

Figure 4. FR-4 FLIR test results.

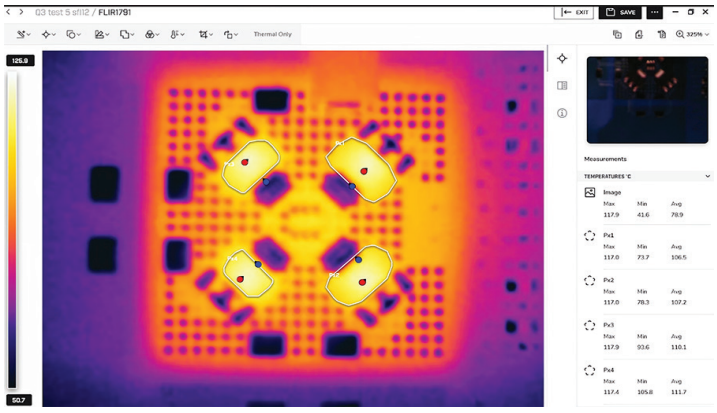

Figure 5. SFL-12 FLIR test results.

Across all validation trials, the average temperature difference between the IR camera and thermocouple measurements was approximately 4°C, with the IR camera consistently reporting temperatures 2°C – 5°C higher than the thermocouples. This systematic offset is consistent with known differences between non-contact IR measurements and direct-contact sensors and is commonly attributed to factors such as assumptions about surface emissivity, sensor contact resistance and localized heat spreading at the measurement point. Importantly, the magnitude of this offset remained stable across test runs and did not vary with substrate material or SMTB configuration.

Because the offset between measurement techniques was both small and consistent, the infrared thermography data is considered reliable for comparative analysis of thermal performance. Relative temperature differences between FR-4 and high-thermal dielectric boards, as well as between SMTB configurations, were preserved across both measurement methods. As a result, the reported temperature reductions, particularly the 26°C baseline difference observed between substrates, are significantly larger than the measurement uncertainty and therefore represent true, material-driven thermal performance improvements rather than measurement artifacts **(Figure 6)**.

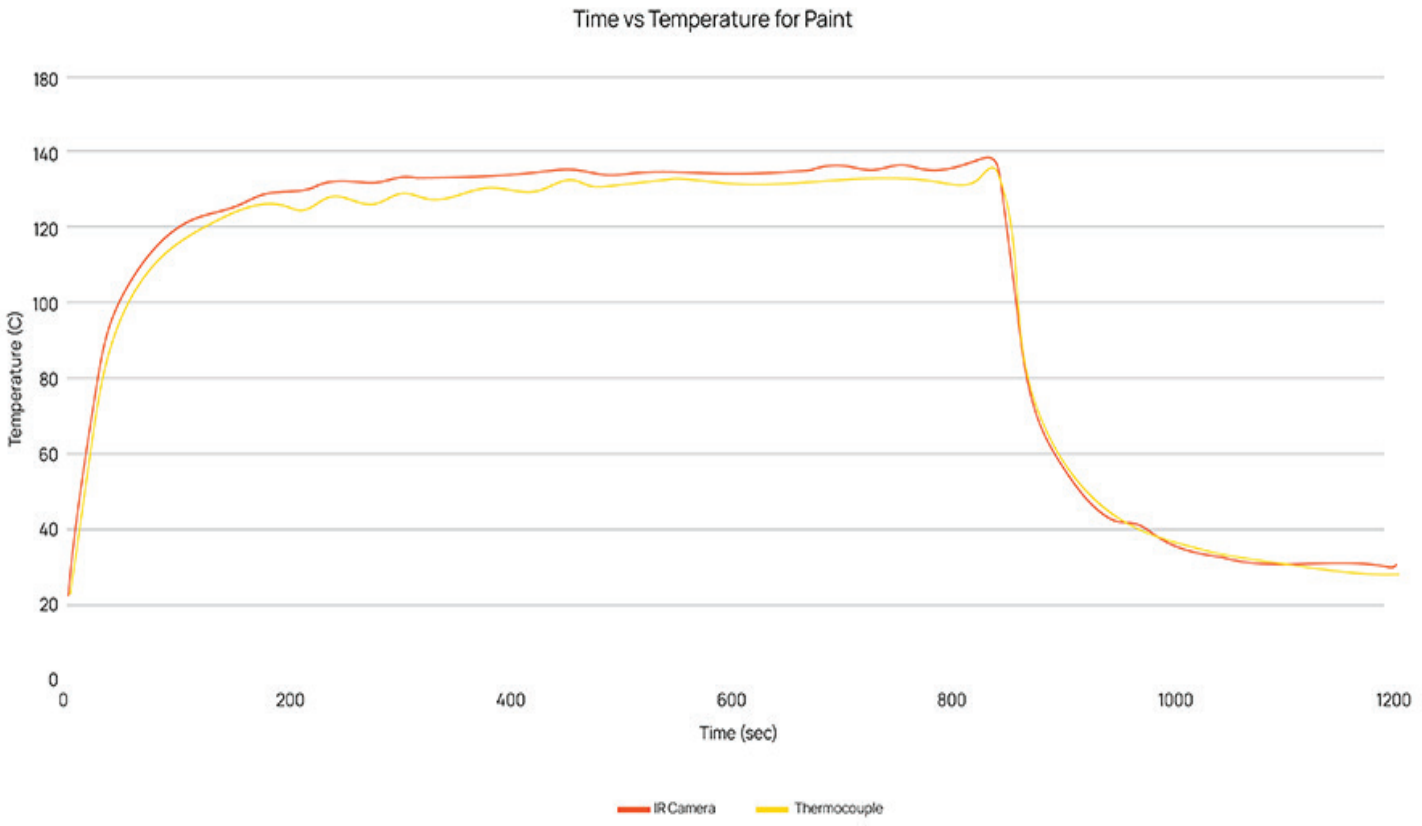

Figure 6. Time-temperature response under power cycling.

Results

Quadrant 1 results: Impact of advanced high-thermal dielectric materials. A direct comparison between FR-4 and the high-thermal dielectric material was performed in quadrant 1, where no surface-mount thermal bridges were present. Under identical operating conditions, infrared measurements showed a maximum component temperature of approximately 144°C on the FR-4 test board **(Figure 7)** compared to approximately 118°C on the high-thermal dielectric test board (Figure 8), resulting in a temperature reduction of 26°C.

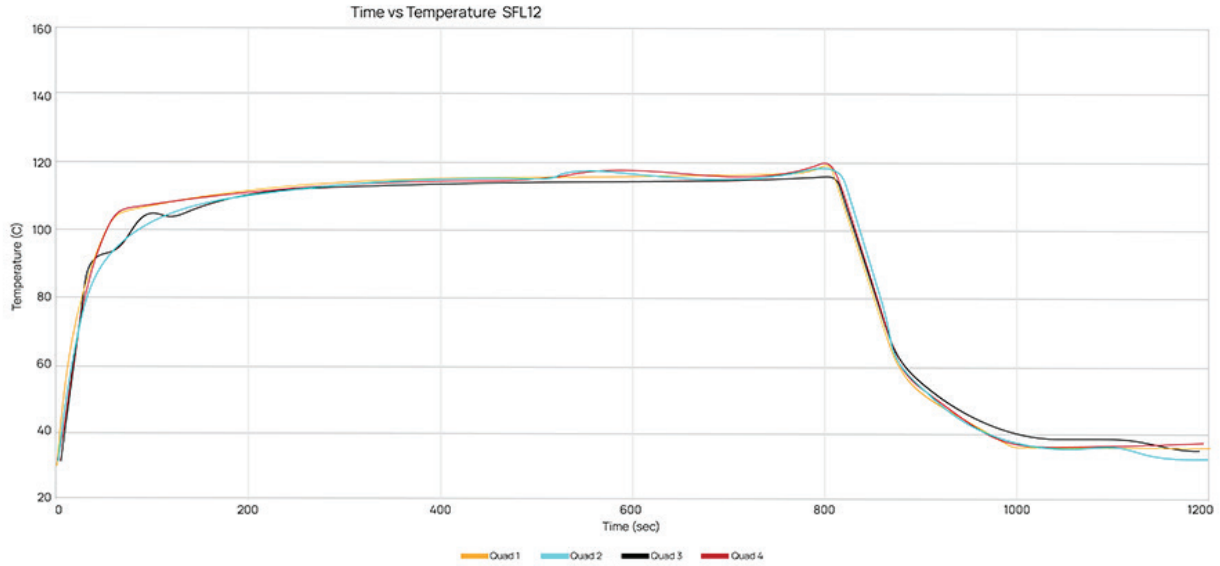

Figure 7. Time-temperature comparison across FR-4 test configurations.

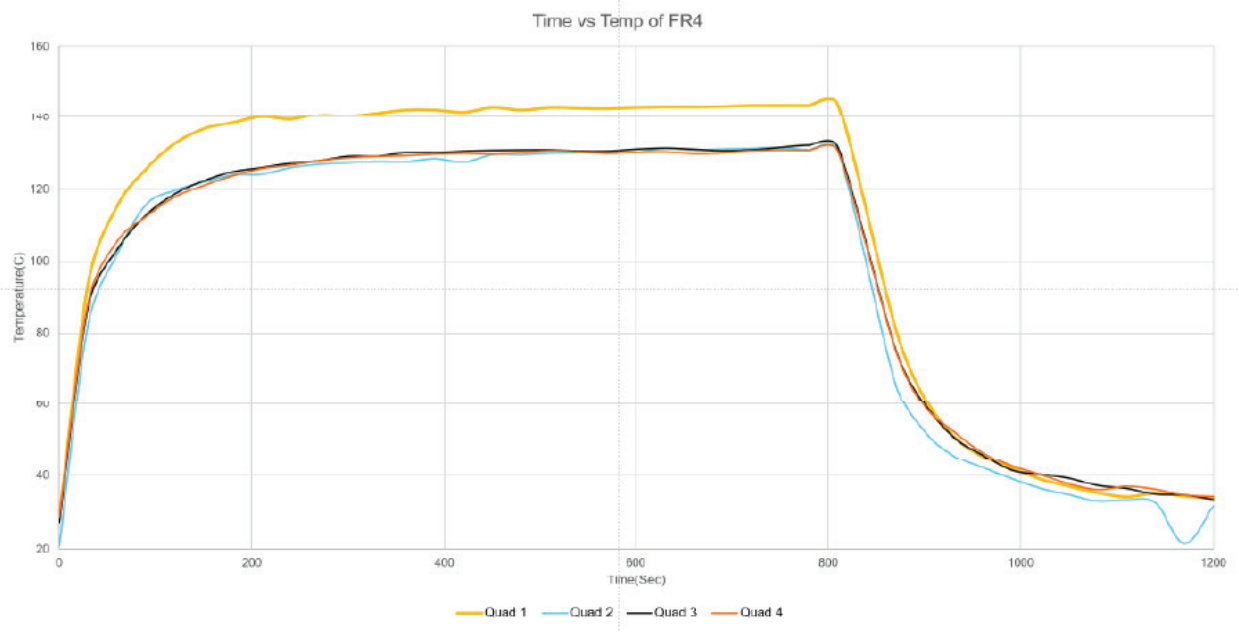

Figure 8. Time-temperature response for SFL-12 high-thermal dielectric test boards.

This result highlights the direct impact of increased dielectric thermal conductivity, approximately 12 W/m·K, on heat dissipation at the component level. The significant reduction in peak temperature demonstrates that improved bulk heat spreading within the PCB stackup alone can substantially lower device operating temperatures, even in the absence of additional localized thermal management features.

Quadrants 2–4 results: impact of SMTBs. Results from quadrants 2 through 4, which incorporated surface-mount thermal bridges, show a consistent reduction in peak component temperature on the FR-4 test boards compared to quadrant 1, where no SMTBs were present. Across the different SMTB sizes evaluated, the FR-4 boards exhibited similar thermal performance, with an average temperature reduction of approximately 14°C relative to the no-bridge condition. These results indicate that, within the tested power range, SMTB size had a limited influence on peak temperature reduction and that the presence of an SMTB itself was the dominant factor.

In this test configuration, two SMTBs were installed per quadrant. Additional experiments conducted with only one SMTB per quadrant showed a smaller temperature reduction of approximately 5°C. Based on these observations, it is reasonable to infer that each SMTB contributed roughly 5°C of peak temperature reduction on the FR-4 substrate. This finding suggests that SMTBs can be an effective localized thermal management strategy for FR-4-based designs operating near their thermal limits, where incremental reductions in component temperature can meaningfully improve design margin.

In contrast, the high-thermal dielectric test boards exhibited a significantly different response to the addition of SMTBs. Across quadrants 2 through 4, the average temperature reduction associated with SMTB use was approximately 2°C. This reduced impact indicates that bulk heat spreading provided by the high-thermal-dielectric material dominated the system's thermal behavior, diminishing the relative contribution of localized heat-spreading elements. These results demonstrate that, while SMTBs can provide measurable benefit on lower-conductivity substrates, their effectiveness is strongly dependent on the underlying dielectric material and becomes less pronounced as intrinsic PCB thermal performance improves.

Conclusion

This study demonstrates that material-level thermal performance within the PCB stackup plays a decisive role in managing heat in power-dense electronic designs. Under controlled, repeatable test conditions, six-layer PCBs fabricated with a high-thermal-dielectric material consistently operated at substantially lower temperatures than equivalent FR-4 boards.

In the baseline configuration without surface-mount thermal bridges, the high-thermal dielectric board exhibited a 26°C reduction in peak component temperature compared to FR-4 (Table 1), clearly illustrating

the impact of increased through-plane thermal conductivity on heat removal at the component level. This result confirms that improved bulk heat spreading within the PCB alone can significantly reduce junction and case temperatures without changes to copper geometry or board architecture.

Key Measurements	FR-4	SFL-12
Peak Temperature Q1	144°C	118°C
Peak Temperature Q2-Q4	130°C	116°C
Delta Temperature with SMTBs	14°C	2°C
Delta Temperature between Substrates	26°C	26°C

Table 1. Key Measurements of Both Test Board Types at Various Locations

The study further shows that surface-mount thermal bridges can provide meaningful localized temperature reductions on conventional FR-4 substrates. In quadrants 2 through 4, the addition of SMTBs reduced peak temperatures on FR-4 boards by 14°C when two bridges were used.

These findings indicate that SMTBs can be an effective mitigation strategy for FR-4-based designs operating near their thermal limits, where incremental reductions in component temperature can improve design margin and reliability. SMTB size had a limited influence within the tested power range, however, suggesting that the presence of a thermal bridge is more critical than its specific form factor under these conditions.

In contrast, the high-thermal dielectric boards exhibited only a modest additional temperature reduction of approximately 2°C with SMTBs. This diminished impact indicates that once bulk heat spreading through the PCB stackup is significantly improved, localized heat-spreading elements provide only incremental benefit.

Together, these results support a substrate-first thermal design approach, in which advanced high-thermal dielectric and prepreg materials serve as the primary mechanism for reducing peak temperatures, while SMTBs function as a complementary, fine-tuning solution for managing residual hotspots. For circuit board designers facing increasing power density and constrained form factors, these findings validate high-thermal dielectric materials as effective drop-in replacements for FR-4 and provide practical guidance on when SMTBs offer the greatest value within an overall PCB thermal management strategy.